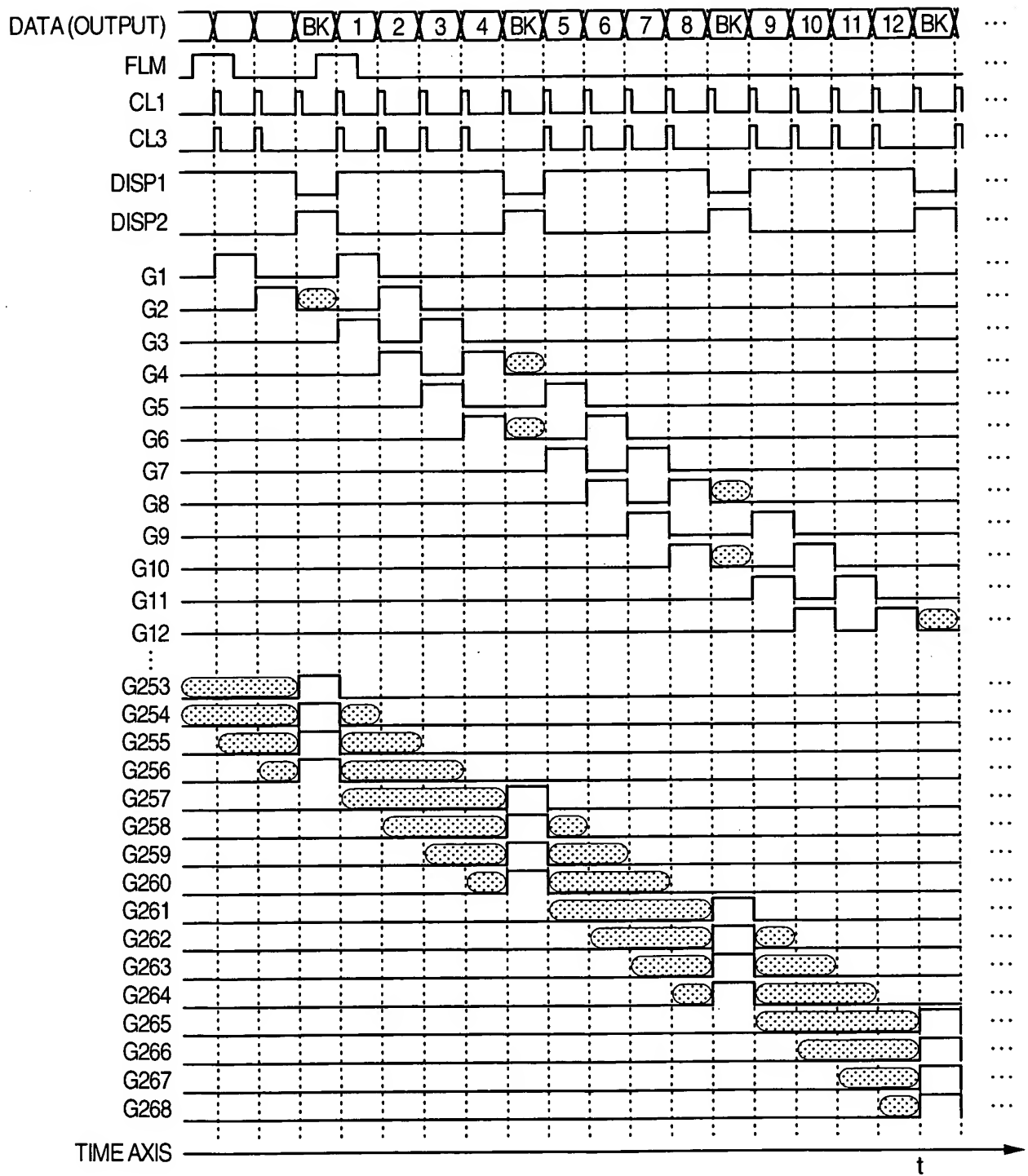
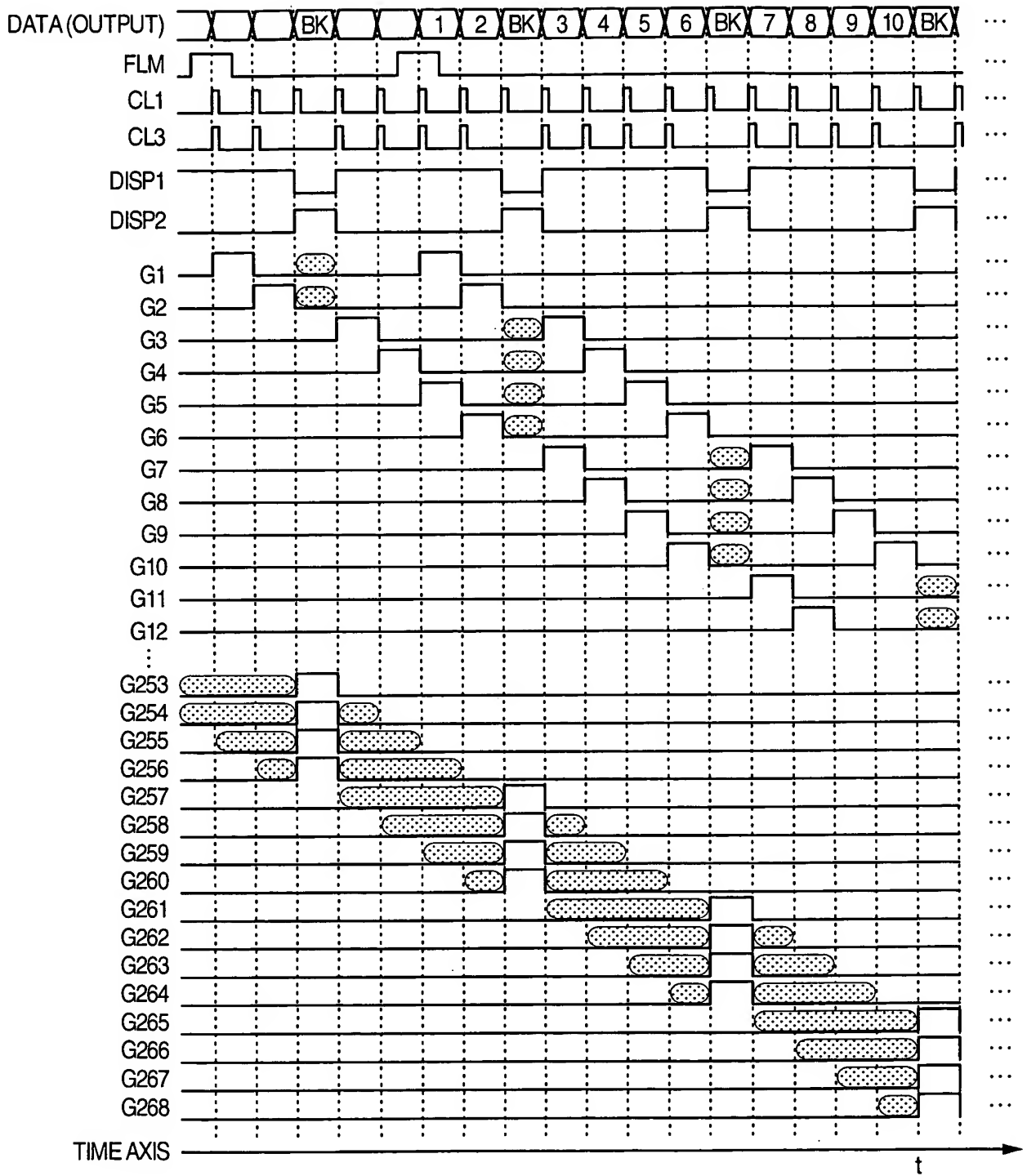


The circuit diagram illustrates a pixel array 101. A Timing Controller 105 provides signals to a Scan Driver 104 and a Data Driver 103. The Scan Driver 104 drives the gate lines G1, G2, G3, ..., Gn. The Data Driver 103 drives the data lines D1R, D1G, D1B, SW, and DmB. Each pixel 101 consists of a switching transistor (SW) controlled by a gate signal from the Scan Driver 104 and a data input from the Data Driver 103. The switching transistor is connected to a common source line Vcom and a pixel electrode (PIX). The pixel electrode is connected to a liquid crystal capacitor (LC) and a storage capacitor (CT), which are both connected to the data line. The pixel array is divided into columns corresponding to red (D1R), green (D1G), blue (D1B), and dummy (DmB) data lines.

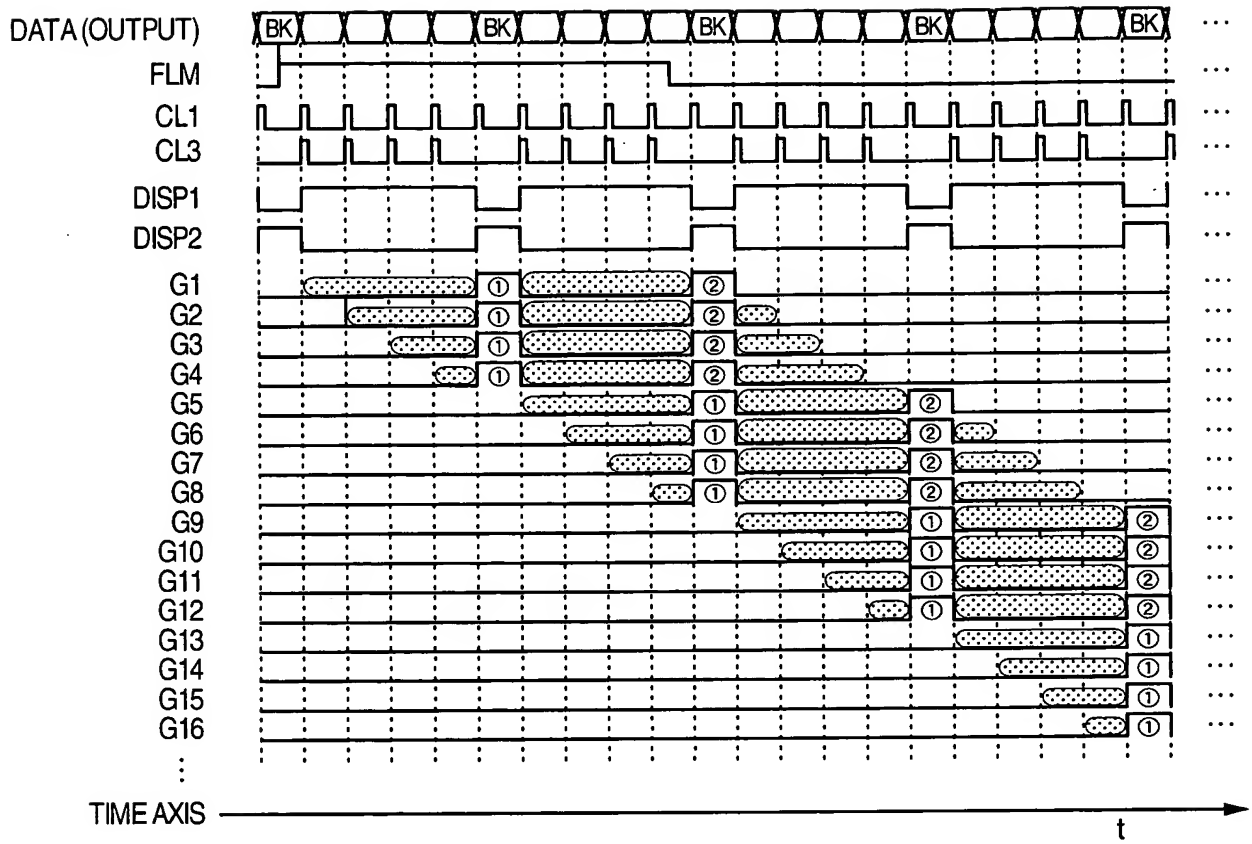
# FIG.3



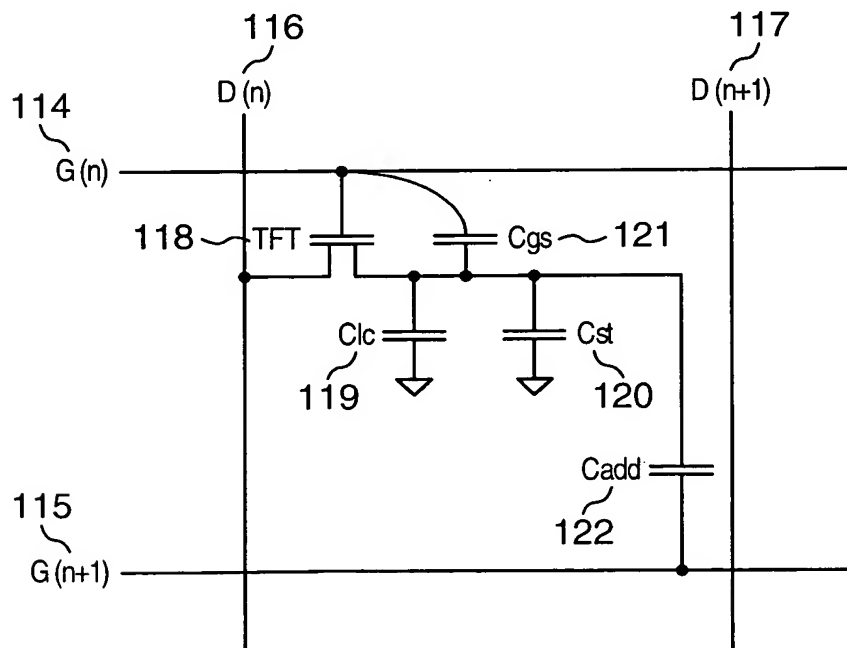
# FIG.4



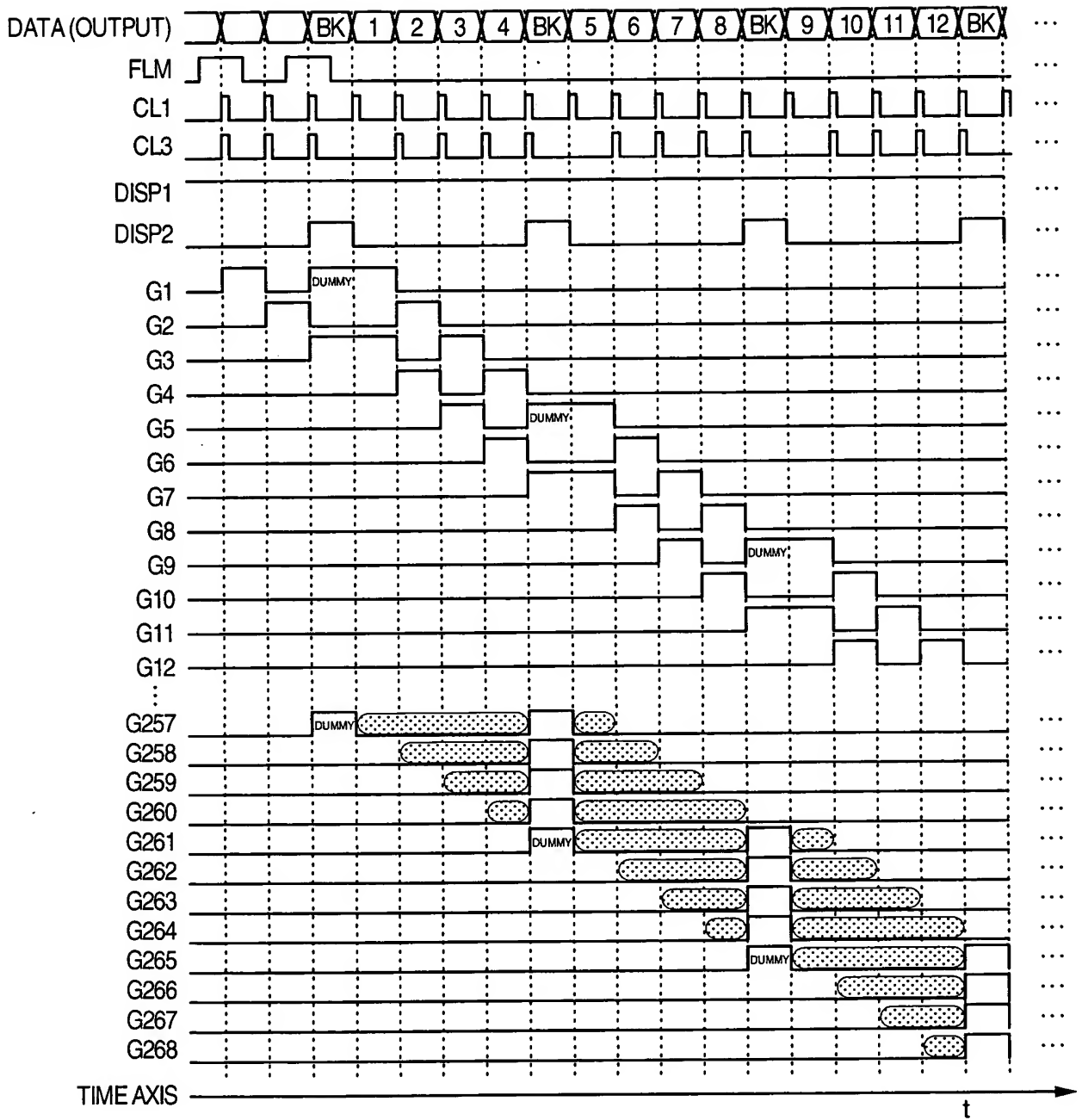
# FIG.5



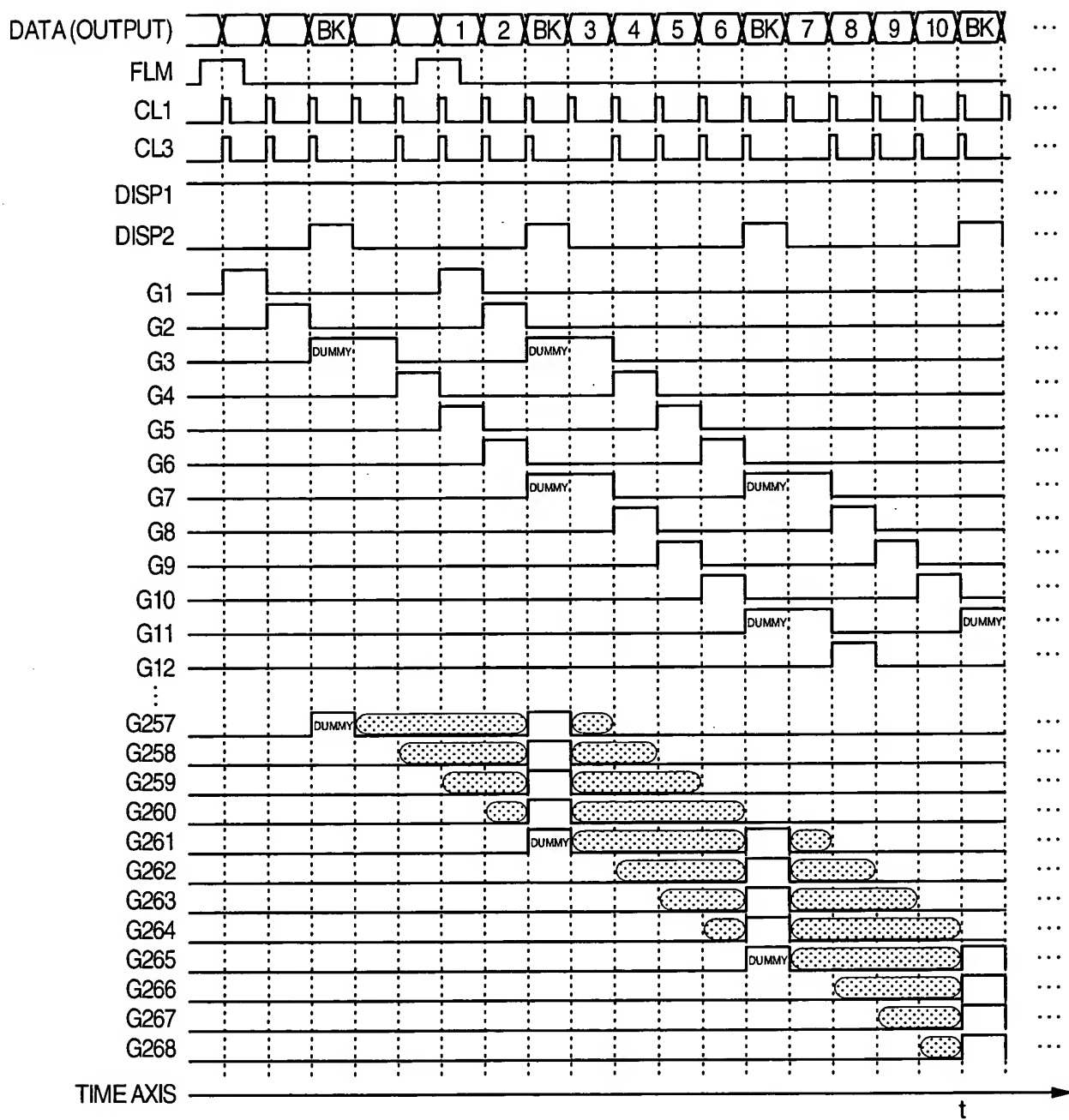
# FIG.6



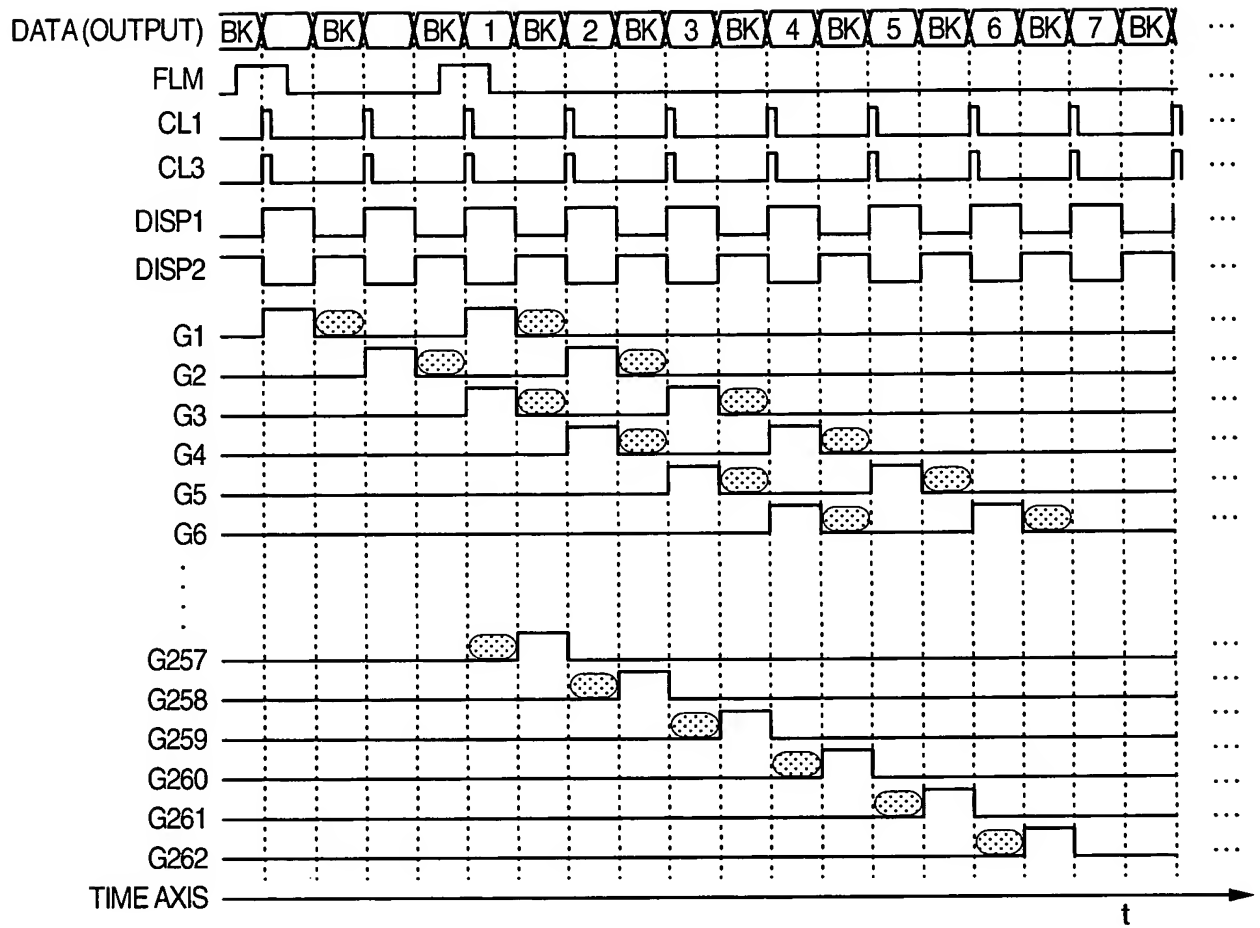
# FIG.7



# FIG.8



# FIG.9



# FIG.10

